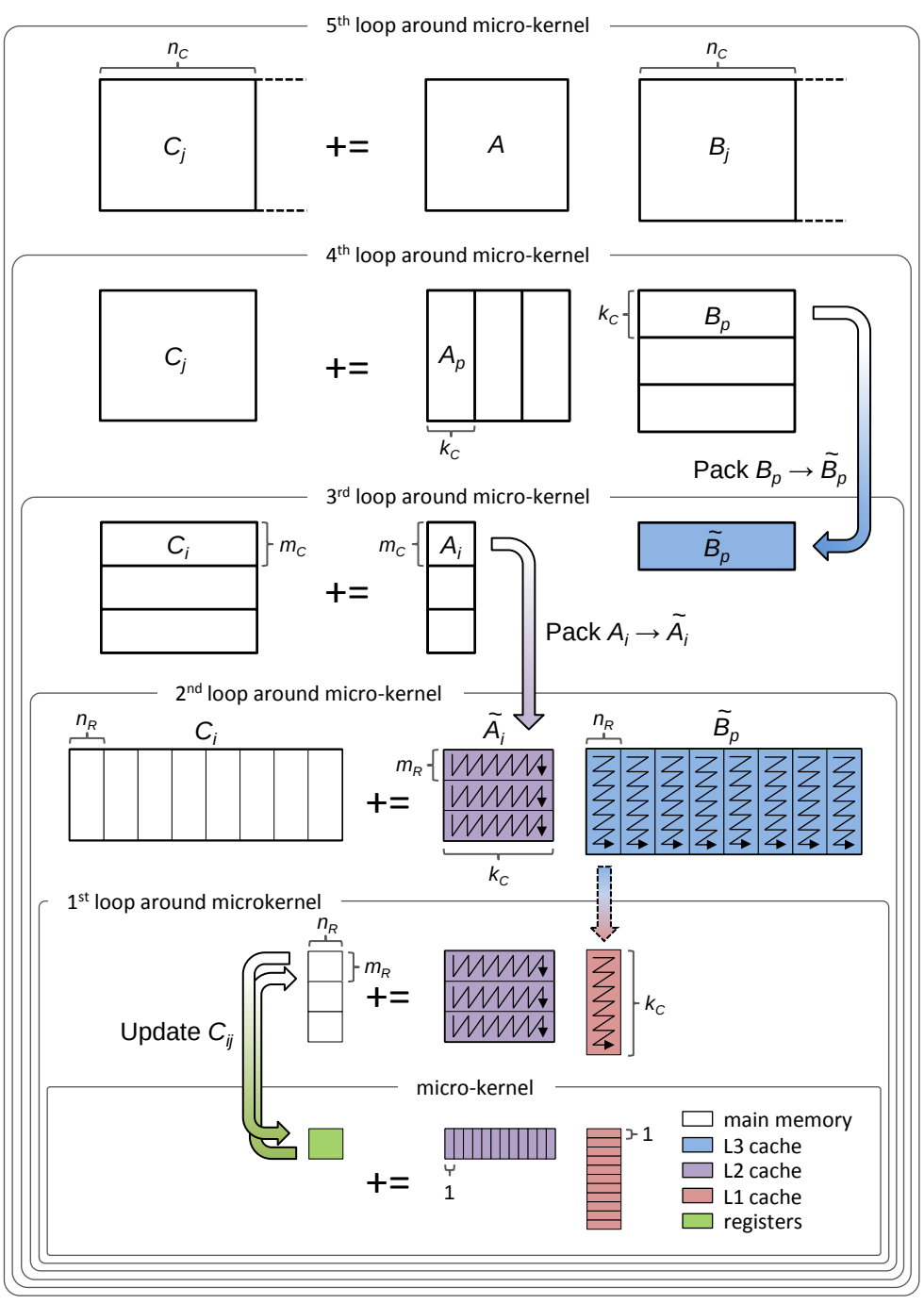
5th loop around micro-kernel
$n_C$
$C_j$
+=
$A$
$n_C$
$B_j$
4th loop around micro-kernel
$C_j$
+=
$A_p$
$k_C$
$k_C$
$B_p$
Pack $B_p \rightarrow \tilde{B}_p$
$\tilde{B}_p$
3rd loop around micro-kernel
$C_i$
$m_C$
+=
$m_C$
$A_i$
Pack $A_i \rightarrow \tilde{A}_i$
2nd loop around micro-kernel
$n_R$
$C_i$
+=
$\tilde{A}_i$
$m_R$
$k_C$
$n_R$
$\tilde{B}_p$
1st loop around microkernel
$n_R$
$m_R$
+=
$k_C$
Update $C_{ij}$
micro-kernel
+=
1
1
main memory
L3 cache
L2 cache
L1 cache
registers